

The diagram shows a system architecture. On the left, a component labeled 10 is connected to a module housing 12. Inside the housing 12, there is a data channel 14 and a termination impedance controller 16. The data channel 14 contains an interface translation block. A signal path is shown from 10 through a resistor 26, a switch 30, and another resistor 32 to the interface translation block. The termination impedance controller 16 is connected to the data channel 14 and provides a control voltage V_{CNTL} . On the right, the module housing 12 is connected to a host device 20. The host device 20 contains a host device interface 24, which is connected to the data channel 14 through a resistor 28 and a switch 34. A control signal 36 is also shown entering the host device interface 24.

FIG. 2

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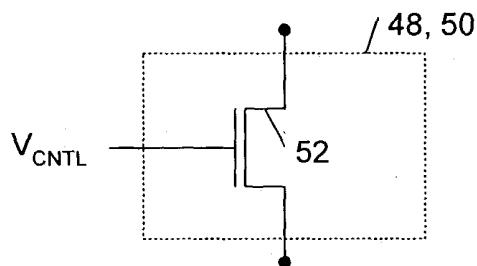


FIG. 3A

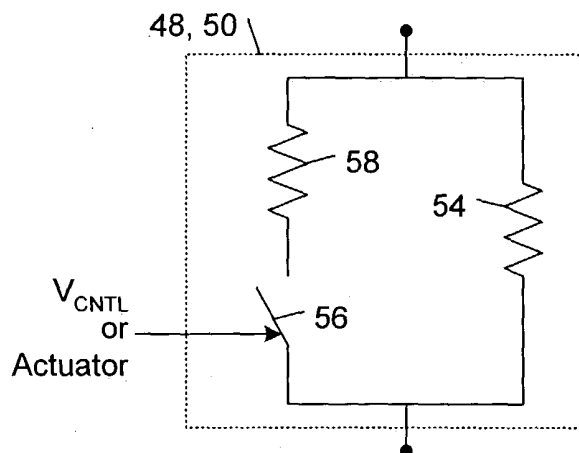


FIG. 3B

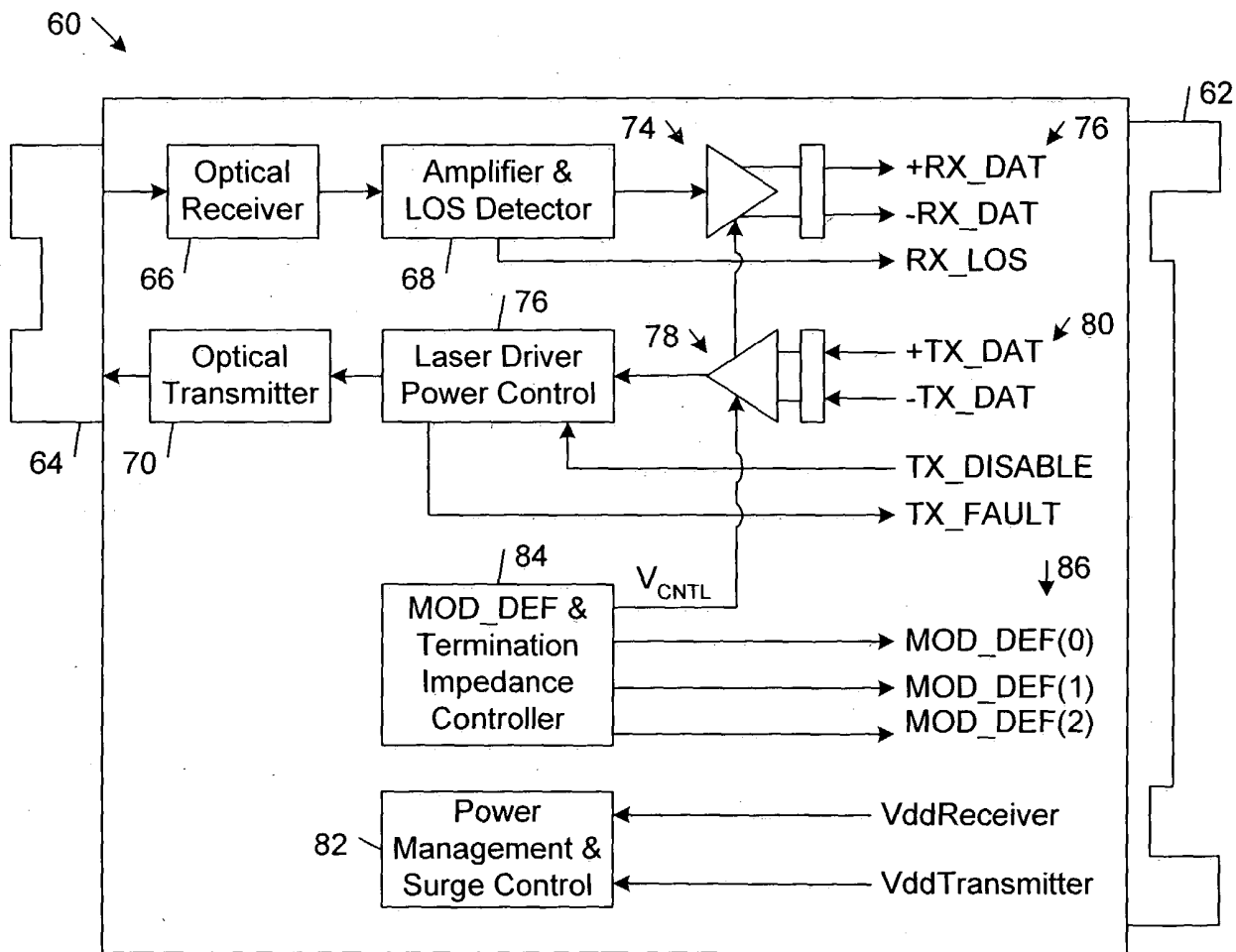


FIG. 4

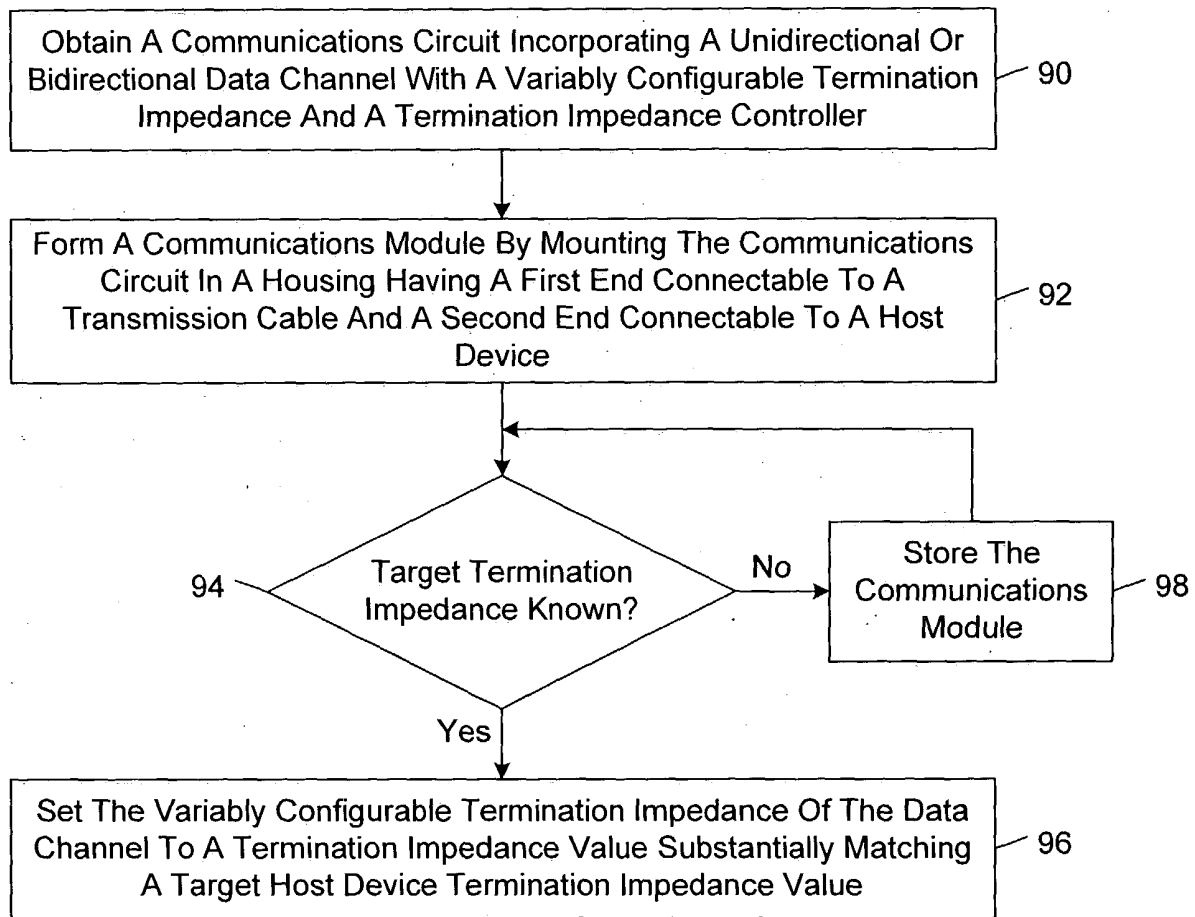


FIG. 5